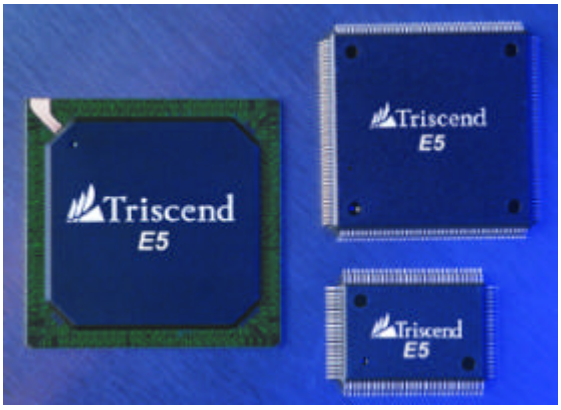
Triscend E5 Configurable Processor Family

October 1998 **Product Brief** (Advance Information)

- **Industry's first complete Configurable Processor System Unit (CPSU)**
  - High-performance, industry-standard "turbo" 8032 microcontroller (10 MIPS at 40 MHz)
  - Up to 64Kbytes of on-chip, dedicated system RAM
  - Up to 3,200 Configurable System Logic (CSL) cells (up to 60,000 gates)
  - High-performance dedicated internal bus
  - Advanced system debug capability
  - Stand-alone operation from a single external memory (code + configuration)
  - Advanced four-layer metal, 0.35µ CMOS process technology, 3.3 volt with 5 volt-tolerant I/O
- **High-performance, industry-standard 8032 "Turbo" embedded microcontroller**
  - Binary and source code compatible with other 8032/8052 variants
  - Three 16-bit timer/counters with programmable modes
  - Bit addressable internal RAM



  - Programmable, full duplex asynchronous serial communications port
  - Numerous programmable I/O (PIO) ports
  - Two-level programmable interrupts
    - 2 external, or from programmable logic
    - 10 internal, including watch-dog timer, software and hardware breakpoints, and DMA transfer
  - Protected watch-dog timer

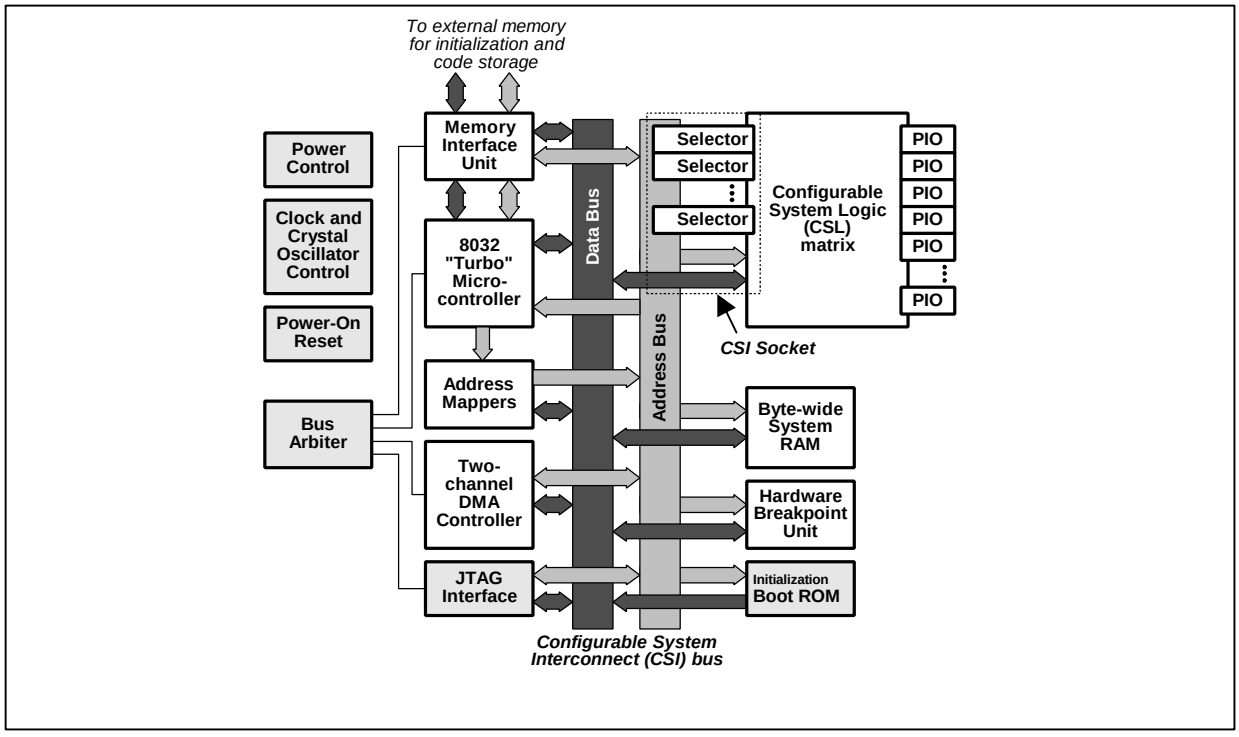


Figure 1. Block Diagram of the Triscend E5 Configurable Processor System Unit (CPSU)

Table 1. Triscend E5 Configurable Processors, Future CPSU Families

Product Family Name	Bit Width	Embedded Processor Core	Device Name	Configurable System Logic cells	System RAM	PIO (max)	Packages
E5	8	40 Mhz, 10 MIPS "TURBO" 8032	TE505S08	512	8Kx8	123	100TQFP, 208QFP
			TE512S16	1152	16Kx8	187	100TQFP, 208QFP
			TE520S40	2048	40Kx8	251	208QFP, 420BGA
			TE532S64	3200	64Kx8	315	208QFP, 420BGA
TBA	32	RISC	(TBA--to be announced)				
TBA	32	CISC	(TBA--to be announced)				

- **Embedded support functions**
  - 2-channel DMA controller
  - IEEE 1149.1 enhanced JTAG interface
  - In-system debug/breakpoint unit
  - Power-on reset
  - Memory Interface Unit (MIU) for flexible, glue-less interface to external memory
  - Power-down and power-management modes
- **Embedded SRAM-based Configurable System Logic matrix**
  - Over 3,800 flip-flops and 300 programmable inputs and outputs (PIOs)
  - Abundant, flexible interconnect structure with easy access to and from system bus
  - Dedicated circuitry for fast adders, counters, and multipliers
  - CSL cells can be configured as memory, including true dual-port operation
  - 6 independent low-skew clock or global signal distribution buffers (in addition to system clock)
- **High performance dedicated system bus**
  - Configurable System Interconnect (CSI) bus integrates CPSU operation
  - Up to 40 Mbytes per second transfer rate
  - 32-bit address bus and 8-bit data bus
  - CSI Socket is openly defined CSI bus interface to CSL matrix
    - Soft peripheral logical addresses stay independent of placement in CSL matrix
    - All soft peripherals forward compatible to future CPSU families
  - Three bus masters and built-in arbitration
    - 8032 microcontroller
    - DMA controller
    - JTAG interface
  - Programmable wait-state support
  - DMA request and acknowledge
- **FastChip™ Development System**
  - Graphical, easy-to-use integrated development environment
  - Library of drag-and-drop soft modules provides microprocessor “derivatives on demand”
  - Seamless interfaces to popular processor development/debug environments
  - Easily import custom logic created with popular schematic capture or logic synthesis packages
  - Logic module generators automatically create optimized functions
  - Automatically creates a configuration file for external memory
  - Real-time in-system debugging support through JTAG interface

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